GAU 1765

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To: Commissioner of Patents and Trademarks
Washington, D.C. 20231

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Subject: Serial No. 09/247,974 02/11/99

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A KEY-HOLE FREE PROCESS FOR HIGH ASPECT RATIO GAP FILLING WITH REENTRANT SPACER

Grp. Art Unit: 1765

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56. Copies of each document is included herewith.

U.S. Patent 5,814,564 to Yao et al., "Etch Back Method to Planarize an Interlayer having a Critical HDP-CVD Deposition Process", shows an etch back method to planarize an interlayer having a critical HDP-CVD deposition process.

U.S. Patent 5,756,396 to Lee et al., "Method of Making a Multi-Layer Wiring Structure having Conductive Sidewall Etch Stoppers and a Stacked Plug Interconnect", teaches full spacers on metal line sidewalls.

U.S. Patent 5,262,352 to Woo et al., "Method for Forming an Interconnection Structure for Conductive Layers", describes a method for forming spacers on metal line sidewalls.

U.S. Patent 5,462,893 to Matsuoka et al., "Method of Making a Semiconductor Device with Sidewall Etch Stopper and Wide Through-Hole having Multilayered Wiring Structure", shows a spacer used as an etch stop on a metal line.

Sincerely,

Stephen B. Ackerman,
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